LEVEL III

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CALIFORNIA INSTITUTE OF TECHNOLOGY

PASADENA, CALIFORNIA 91125

COMPUTER SCIENCE 256-80

R&D STATUS REPORT

ARPA ORDER NO. 3771 Amend. No. 1 (11) 1 Dec 80

CONTRACTOR: Caltech

CONTRACT NUMBER: (15) N00014-79-C-0924, ARPA Order-3771

EFFECTIVE DATE OF CONTRACT: September 1, 1979

EXPIRATION DATE OF CONTRACT: October 15, 1980

PRINCIPAL INVESTIGATOR: (10) Carver Mead

(12) 4

TELEPHONE NUMBER: (213) 356-6811

SHORT TITLE: (6) Demonstration of the Use of VLSI Design Rules, Standards, and Interfaces.

REPORTING PERIOD: September 1, 1980 to December 1, 1980

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(9) Research and development status rpt, 1 Sep-1 Dec 80

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DESCRIPTION OF PROGRESS

Progress is reported for each element of Tasks 1, 2 and 3.

TASK 1

1. Consultation from Fabrication Lines

Final written reports were received from Honeywell and Hughes. The results of their evaluation were known previously and have already been incorporated in the test-chip design and design rule considerations.

2. CMOS-SOS and NMOS-Si Gate Test-Chips

The revised NMOS test-chip was fabricated as part of MPC880. Chips have been recieved at JPL and some limited measurements have been made. A final version of the NMOS test-chip design is now underway and is expected to be completed in January. Additional inputs from the contractors reports and from NBS and NSA have been taken into account.

The design of the JPL CMOS-SOS Test-Chip No. 1 (SOSONE) and the Test-Strip have been completed. SOSONE is a drop-in test-chip of 6mm X 6mm dimensions. The test-strip consists of four 2 X 10 pad arrays and is designed to be incorporated into every chip of the fabrication run. This version of SOSONE consists of seven different types of random fault arrays, one parametric device area and one "canary" circuit.

The design of a second SOS test chip (SOSTWO) has also been completed. This chip is smaller than SOSONE and consists of four different types of random fault arrays and one parametric device area consisting of crossbridge and contact resistors of varying dimensions.

3. Geometrical Design Rules

Design rules for NMOS and CMOS-SOS have been finalized. Documentation describing these rules exists for both.

4. Speed and Timing Rules

The final report is in the process of being revised (see last quarterly report).

5. CIF

Work complete; no further progress.

6. Testability Rules

Work is proceeding - See last quarterly report.

TASK 2

1. Design-Rule Checker

Deleted (see last quarterly report).

2. CIF/APPLICON, CALMA Conversion Software

The software development for converting CIF to APPLICON has proceeded. The task is about 90% complete.

3. Circuit Design

The corrected memory interface building block design was fabricated as part of MPC880. Chips have been received and tested. The circuit was found to perform normally under static operation.

The design of the CMOS-SOS version of the memory interface chip has been completed. It is now awaiting fabrication by Task 3.

An extension of the ART design program called CART has been completed. CART is a collection of Pascal procedures which provide a means of generating a CIF file for CMOS-SOS. This program defines seven specific layers and makes possible the design of 4-terminal structures. It was used to generate the CIF files for all of the JPL and NBS CMOS-SOS chips designed as part of this program.

TASK 3

1. Contract Negotiations

Negotiations with Hughes and Rockwell for the fabrication of CMOS-SOS circuits were initiated. Discussions centered around terms and conditions, management approvals, and technical agreements.

2. Fabrication

Fabrication will begin after contract negotiations are completed.

CHANGES IN KEY PERSONNEL: none

SUMMARY OF SUBSTANTIVE INFORMATION DERIVED FROM SPECIAL EVENTS: none

PROBLEMS ENCOUNTERED OR ANTICIPATED: none

ACTION REQUIRED BY THE GOVERNMENT:

A formal request has been made to extend the expiration date of the contract to August 31, 1981 because of delays in securing CMOS-SOS fabrication. Work has been proceeding accordingly.

FISCAL STATUS:

1.	Amount currently on contract:		$630,718
2.	Expenditures and commitments to date:		
	Campus Salaries and Contracts:	12,802	
	JPL Salaries and Contracts:	470,651	
			$483,453
3.	Funds required to complete all Tasks:		$147,265

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